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EXAMINER	
RYMAN, DANIEL J	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/621,315	SIKKINK ET AL.	
	Examiner	Art Unit	
	Daniel J. Ryman	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-10,14-16 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-10,14-16 and 18* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the Appeal Brief filed on 3 March 2006, PROSECUTION IS HEREBY REOPENED. A rejection set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

2. Applicant's arguments with respect to claims 1, 3-6, 8-10, 14-16, and 18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claim 1 is objected to because of the following informalities: in line 2, "at by a" should be "by a". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-6, 8, 9, 15, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs (USPN 5,909,563) in view of Duffy (USPN 6,535,527), of record, in further view of Santahuhta (EP 0989484), of record, in further view of Khandekar et al. (USPN 6,049,887), of record.

6. Regarding claim 1, Jacobs discloses an interface (ref. 106) for data transfer from a first domain (ref. 102) clocked by a first clock at a first frequency to a second domain (ref. 104) clocked by a second clock at a slower frequency (col. 1, line 66-col. 2, line 6 and col. 2, lines 52-55), comprising: a first register (ref. 112) for receiving data from the first domain when the first register is selected (Figs. 3 and 4 and col. 3, lines 12-16); a second register (ref. 112) for receiving data from the first domain when the second register is selected (Figs. 3 and 4 and col. 3, lines 12-16); and a third register (ref. 118) for transferring data from said first register or said second register to the second domain when the second domain is clocked by a clock pulse of the second clock (col. 3, lines 31-39), said third register being selectively toggled to receive data from said first register or said second register upon a clock pulse (see col. 3, lines 31-39 where a multiplexer toggles the third register); wherein the first and second registers are clocked at the first clock at the first clock frequency (Figs. 3 and 4 and col. 3, lines 12-16); and wherein the first clock clocking the first domain and the second clock clocking the second domain generate pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse (SYNC signals) (col. 1, line 66-col. 2, line 6 and col. 2, line 66-col. 3, line 6).

Jacobs does not expressly disclose that the registers are latches; however, it is well known in the art to use latches for registers, as is evidenced by Duffy (col. 3, line 49-col. 4, line

9). In addition, Santahuhta teaches that the difference between a latch and a register is that latches are set to have data written on the rising edge of a clock signal and to have data read on the falling edge of a clock signal where a register records data according to a set input signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the registers comprise latches since using latches to construct registers is very well known in the art. In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to use latches for the registers since the registers in Jacobs read and write data according to a clock signal where latches read and write data according to a clock signal.

Further, Jacobs in view of Duffy does not expressly disclose that the third latch is selectively toggled in response to a negative edge of the clock pulse clocking the second domain; however, Jacobs in view of Duffy does disclose that the third latch is selectively toggled in response to a clock pulse from a processor clock (Jacobs: col. 3, lines 31-37). Santahuhta teaches, in a system for synchronizing a data stream, selectively toggling the read of two latches in response to a negative edge of the clock pulse clocking the second domain (col. 4, lines 33-48 and col. 5, lines 21-39) where the toggling is controlled by a processor with a clock input (Fig. 3, ref 304; Fig. 4, ref. 106 and 107; col. 2, line 54-col. 3, line 13; and col. 4, lines 33-48) since a latch has data read from it on the falling edge of a clock signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the third latch be alternately toggled in response to a negative edge of the clock pulse clocking the second domain since latches have data read from them on the falling edge of a clock signal.

Jacobs in view of Duffy in further view of Santahuhta does not expressly disclose that the first clock and the second clock are both derived from a single primary clock or that the secondary synch pulse is generated by the same primary clock. Khandekar teaches, in a system for transferring a signal between two synchronous clock domains, having a first clock clocking a first domain and a second clock clocking the second domain be both derived from a single primary clock (Figs. 3 and 5, common oscillator) in order to ensure that both clock domains are synchronized (col. 1, lines 35-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to generate the first and second clocks by using a single primary clock and to generate the secondary synch signal using the primary clock in order to ensure that the clocks are synchronized.

7. Regarding claim 3, Jacobs in view of Duffy in further view of Santahuhta in further view of Khandekar suggests that at least one clock pulse of the first domain clock is a non-operate (NOP) clock pulse in each repeated systematic pattern when no data from the first domain is loaded into either said first latch or said second latch to cause equal average data transfer between the first domain and the second domain (Santahuhta: col. 6, lines 14-46).

8. Regarding claim 4, Jacobs in view of Duffy in further view of Santahuhta in further view of Khandekar suggests that the NOP clock pulse is selected to minimize latency and prevent the slower clocked domain from being overrun by the faster clocked domain (Santahuhta: col. 6, lines 14-46).

9. Regarding claim 5, Jacobs in view of Duffy in further view of Santahuhta in further view of Khandekar discloses that the first and second latches are alternately selected by a select signal,

said select signal being generated to select one of said first or second latches when the other of said first or second latches receives data (Jacobs: col. 3, lines 12-30).

10. Regarding claim 6, Jacobs discloses an interface (ref. 106) for data transfer between a first domain (ref. 102) clocked at one frequency and a second domain (ref. 104) clocked at a faster frequency (col. 1, line 66-col. 2, line 6 and col. 2, lines 52-55) where Jacobs allows for the first domain to be either faster or slower than the second domain, comprising: a first register (ref. 112) for receiving data from the first domain when the first register is selected (Figs. 3 and 4 and col. 3, lines 12-16); a second register (ref. 112) for receiving data from the first domain when the second register is selected (Figs. 3 and 4 and col. 3, lines 12-16); and a third register (ref. 118) selectively toggled to receive data from said first register or said second register upon a clock pulse, other than a hold pulse (see col. 3, lines 31-39 where a multiplexer toggles the third register) where Jacobs has no hold pulse such that every clock pulse is "other than a hold pulse", said third register transferring data from said first latch or said second register to the second domain when the second domain is clocked by a next clock pulse that is not a hold clock pulse (col. 3, lines 31-39); and wherein the first clock clocking the first domain and the second clock clocking the second domain generate pulses that repeat in a ratioed, systematic pattern framed by a secondary synch pulse (SYNC signals) (col. 1, line 66-col. 2, line 6 and col. 2, line 66-col. 3, line 6).

Jacobs does not expressly disclose that the registers are latches; however, it is well known in the art to use latches for registers, as is evidenced by Duffy (col. 3, line 49-col. 4, line 9). In addition, Santahuhta teaches that the difference between a latch and a register is that latches are set to have data written on the rising edge of a clock signal and to have data read on

the falling edge of a clock signal where a register records data according to a set input signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the registers comprise latches since using latches to construct registers is very well known in the art. In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to use latches for the registers since the registers in Jacobs read and write data according to a clock signal where latches read and write data according to a clock signal.

Further, Jacobs in view of Duffy does not expressly disclose that the third latch is selectively toggled in response to a negative edge of the clock pulse clocking the second domain; however, Jacobs in view of Duffy does disclose that the third latch is selectively toggled in response to a clock pulse from a processor clock (Jacobs: col. 3, lines 31-37). Santahuhta teaches, in a system for synchronizing a data stream, selectively toggling the read of two latches in response to a negative edge of the clock pulse clocking the second domain (col. 4, lines 33-48 and col. 5, lines 21-39) where the toggling is controlled by a processor with a clock input (Fig. 3, ref 304; Fig. 4, ref. 106 and 107; col. 2, line 54-col. 3, line 13; and col. 4, lines 33-48) since a latch has data read from it on the falling edge of a clock signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the third latch be alternately toggled in response to a negative edge of the clock pulse clocking the second domain, other than a hold pulse, since latches have data read from them on the falling edge of a clock signal.

Jacobs in view of Duffy in further view of Santahuhta does not expressly disclose that the first clock and the second clock are both derived from a single primary clock or that the

secondary synch pulse is generated by the same primary clock. Khandekar teaches, in a system for transferring a signal between two synchronous clock domains, having a first clock clocking a first domain and a second clock clocking the second domain be both derived from a single primary clock (Figs. 3 and 5, common oscillator) in order to ensure that both clock domains are synchronized (col. 1, lines 35-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to generate the first and second clocks by using a single primary clock and to generate the secondary synch signal using the primary clock in order to ensure that the clocks are synchronized.

11. Regarding claim 8, Jacobs in view of Duffy in further view of Santahuhta in further view of Khandekar suggests that the hold clock pulse is selected to minimize latency since the hold clock pulse (reset) delays the second domain data read until data is available to read (Santahuhta: col. 6, lines 14-46).

12. Regarding claim 9, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar discloses that the first and second latches are alternately selected by a select signal, said select signal being generated to select one of said first or second latches when the other of said first or second latches receives data (Jacobs: col. 3, lines 12-30).

13. Regarding claim 15, Jacobs discloses a method for data transfer between clocked domains (refs. 102, 104) (col. 1, line 66-col. 2, line 6 and col. 2, lines 52-55), comprising: loading a first master register (ref. 112) with data from the first domain in response to a first domain clock pulse (Figs. 3 and 4 and col. 3, lines 12-16); transferring the data loaded in the first master register to the second domain through a slave register (ref. 118) in response to a second domain clock pulse (col. 3, lines 31-39); toggling the slave register to switch to receive data from

a second master register (ref. 112) (see col. 3, lines 31-39 where a multiplexer toggles the third register); loading the second master register with data from the first domain in response to another first domain clock pulse (Figs. 3 and 4 and col. 3, lines 12-16); transferring the data loaded in the second master register to the second domain through the slave register in response to another second domain clock pulse (col. 3, lines 31-39); toggling the slave register to switch to receive data from the first master register (see col. 3, lines 31-39 where a multiplexer toggles the third register); repeating a cycle of alternately loading the first and second master registers and transferring data to the second domain through the slave register (col. 3, lines 12-16 and col. 3, lines 31-39); wherein the clock pulses of the first domain and the second domain repeat in a ratioed, systematic pattern framed by a secondary synch pulse (SYNC signals) (col. 1, line 66-col. 2, line 6 and col. 2, line 66-col. 3, line 6).

Jacobs does not expressly disclose that the registers are latches; however, it is well known in the art to use latches for registers, as is evidenced by Duffy (col. 3, line 49-col. 4, line 9). In addition, Santahuhta teaches that the difference between a latch and a register is that latches are set to have data written on the rising edge of a clock signal and to have data read on the falling edge of a clock signal where a register records data according to a set input signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the registers comprise latches since using latches to construct registers is very well known in the art. In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to use latches for the registers since the registers in Jacobs read and write data according to a clock signal where latches read and write data according to a clock signal.

Further, Jacobs in view of Duffy does not expressly disclose that the slave latch is alternately toggled in response to a negative edge of the clock pulse clocking the second domain; however, Jacobs in view of Duffy does disclose that the slave latch is alternately toggled in response to a clock pulse from a processor clock (Jacobs: col. 3, lines 31-39). Santahuhta teaches, in a system for synchronizing a data stream, alternately toggling the read of two latches in response to a negative edge of the clock pulse clocking the second domain (col. 4, lines 33-48 and col. 5, lines 21-39) where the toggling is controlled by a processor with a clock input (Fig. 3, ref 304; Fig. 4, ref. 106 and 107; col. 2, line 54-col. 3, line 13; and col. 4, lines 33-48) since a latch has data read from it on the falling edge of a clock signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the slave latch be alternately toggled in response to a negative edge of the clock pulse clocking the second domain, other than a non-operate clock pulse, since latches have data read from them on the falling edge of a clock signal.

Additionally, Jacobs in view of Duffy does not expressly disclose repeating a cycle of alternately loading the first and second master registers and transferring data to the second domain through the slave register until a master clear signal is received by the slave and master registers; and entering a non-operate state during each repeated cycle for at least one clock pulse of the faster domain clock, if the domains are clocked at different frequencies. Santahuhta teaches, in a system for synchronizing a data stream, repeating a cycle of alternately loading the first and second master registers and transferring data to the second domain through the slave register until a master clear signal (reset) is received by the slave and master registers; and entering a non-operate state during each repeated cycle for at least one clock pulse of the faster

domain clock, if the domains are clocked at different frequencies since the reset is required if not enough data has entered the system when the first domain is slower than the second domain in order to allow the first domain to catch up to the second domain (col. 6, lines 14-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to repeat a cycle of alternately loading the first and second master registers and transferring data to the second domain through the slave register until a master clear signal (reset) is received by the slave and master registers; and enter a non-operate state during each repeated cycle for at least one clock pulse of the faster domain clock, if the domains are clocked at different frequencies since a reset is required if not enough data has entered the system when the first domain is slower than the second domain in order to allow the first domain to catch up to the second domain.

Jacobs in view of Duffy in further view of Santahuhta does not expressly disclose that the first clock and the second clock are both derived from a single primary clock. Khandekar teaches, in a system for transferring a signal between two synchronous clock domains, having a first clock clocking a first domain and a second clock clocking the second domain be both derived from a single primary clock (Figs. 3 and 5, common oscillator) in order to ensure that both clock domains are synchronized (col. 1, lines 35-67). It would have been obvious to one of ordinary skill in the art at the time of the invention to generate the first and second clocks by using a single primary clock in order to ensure that the clocks are synchronized.

14. Regarding claim 16, Huon in view of Duffy in further view of Santahuhta in further view of Khandekar discloses generating a signal in response to loading one of the first or second master latches to cause data to be loaded alternately into the first and second master latches

(Jacobs: Figs. 3 and 4 and col. 3, lines 12-16 and Santahuhta: col. 4, lines 33-48 and col. 5, lines 21-39).

15. Regarding claim 18, Jacobs in view of Duffy in further view of Santahuhta in further view of Khandekar suggests that the non-operate state is selected to minimize latency in transferring the data between the domains since the hold clock pulse (reset) delays the second domain data read until data is available to read (Santahuhta: col. 6, lines 14-46).

16. Claims 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs (USPN 5,909,563) in view of Duffy (USPN 6,535,527), of record, in further view of Santahuhta (EP 0989484), of record.

17. Regarding claim 10, Jacobs discloses an interface (ref. 106) for data transfer between domains (refs. 102, 104) clocked at different frequencies, comprising: a first register (ref. 112) for receiving data from a first domain clocked at one frequency when said first register is selected (Figs. 3 and 4 and col. 3, lines 12-16); a second register (ref. 112) for receiving data from the first domain when said second register is selected (Figs. 3 and 4 and col. 3, lines 12-16); and a third register (ref. 118) for transferring data from either said first register or said second register to a second domain clocked at another frequency (col. 3, lines 31-39), wherein the first domain is clocked at a slower frequency than the second domain (col. 1, line 66-col. 2, line 6 and col. 2, lines 52-55) where Jacobs allows for the first domain to be either faster or slower than the second domain; and wherein said third latch is loaded when the second domain is clocked by a clock pulse that is not a non-operate pulse (col. 3, lines 31-39) where Jacobs has no non-operate pulse such that every clock pulse is "not a non-operate pulse".

Jacob does not expressly disclose that the registers are latches; however, it is well known in the art to use latches for registers, as is evidenced by Duffy (col. 3, line 49-col. 4, line 9). In addition, Santahuhta teaches that the difference between a latch and a register is that latches are set to have data written on the rising edge of a clock signal and to have data read on the falling edge of a clock signal where a register records data according to a set input signal (col. 3, line 25-col. 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the registers comprise latches since using latches to construct registers is very well known in the art. In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to use latches for the registers since the registers in Jacobs read and write data according to a clock signal where latches read and write data according to a clock signal.

18. Regarding claim 14, incorporating the rejection of claim 1, Jacobs in view of Duffy in further view of Santahuhta discloses that the third latch is alternately toggled to transfer data from said first or said second latch in response to a negative edge of a clock pulse clocking the second domain unless the clock pulse is a non-operate clock pulse (Jacobs: col. 3, lines 31-39 and Santahuhta: Fig. 3, ref 304; Fig. 4, ref. 106 and 107; col. 2, line 54-col. 3, line 13; col. 3, line 25-col. 4, line 11; col. 4, lines 33-48; col. 5, lines 21-39; and col. 6, lines 14-46).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Manning (USPN 6,000,022) see col. 6, line 52-col. 7, line 38, esp. col. 7, lines 33-37 which pertains initiating a non-operate pulse to minimize latency. Bryant et al (USPN 6,535,946) see entire document which pertains to synchronizing data transfers between clock domains

derived from a common clock. Rios (USPN 5,256,912) see entire document which pertains to synchronizing data transfers between clock domains. Taylor (USPN 5,758,131) see entire document which pertains to synchronizing data transfers between clock domains.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The examiner can normally be reached on Mon.-Fri. 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel J. Ryman
Examiner
Art Unit 2665

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SUPERVISORY PATENT EXAMINER
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